## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Examiner: Not Yet Assigned
	Art Unit: Not Yet Assigned
Iu-Meng Tom Ho	
Application No.: Not Yet Assigned	"Express Mail CERTIFICATE OF MAILING  "Express Mail" mailing label number: £ \( \frac{336589817 US}{1 \) hereby certify that I am causing this paper or fee to be deposited with
Filing Date: <u>Herewith</u>	the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to Commissioner for Patents, P.O. Box 1450,
For: Power and Ground Mesh to Remove	Alexandria, VA 22313-1450 on:
Capacitive and Inductive Signal Coupling Effects of Routing in	3-26.04 (Date of Deposit)
Integrated Circuit Device	(Name of Person Mailing Correspondence)
	Hathleen K. Mults 3-26-04 (Signature) (Date)

Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450

## INFORMATION DISCLOSURE STATEMENT

## Examiner:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 submitted under 37 C.F.R. §1.97(b). It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to C.F.R. 1.98(d), copies of the references are not being provided herewith since they were previously submitted to, or cited by, the Patent and Trademark Office in the parent application, U.S. Patent Application Serial No. 10/132,996 filed on

April 25, 2002, which application is relied upon for an earlier effective filing date under 35 U.S.C. 120.

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure

Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 3/16, 2009

James C. Scheller, Jr. Reg. No. 31,195

12400 Wilshire Blvd. Seventh Floor Los Angeles, CA 90025-1026 (408) 720-8300

Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)			Attorney Docket No.: 02986.P029C	Application Number:			
					First Named Inventor: Iu-Meng Tom Ho		
					Filing Date:		
-	- 1			U.S. PATEN	T DOCUMENTS		
Exam. Initial*	Cite No. <sup>1</sup>	U.S. Patent Document		N	lame of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (If known)				
		6,348,722		Yoshikoshi		02-19-2002	

OTHER ART – NO PATENT LITERATURE DOCUMENTS					
Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published				
	Magma Design Automation, Inc., "Deep-Submicron Signal Integrity", white paper, 2002				
	Andrey V. Mezhiba, Eby G. Friedman, "Scaling Trands of On-Chip Power Distribution Noise", SLIP'02, April 6-7, 2002, San Diego, California, USA, pp.47-53				
	Sani R. Nassif, Onsi Fakhouri, "Technology Trends in Power-Grid-Induced Noise", SLIP'02, April 6-7, 2002, San Diego, California, USA, pp.55-59				
	Seongkyun Shin, Yungseon Eo, William R. Eisenstadt, Jongin Shim, "Analytical Signal Integrity Verification Models for Inductance-Dominant Multi-Coupled VLSI Interconnects", SLIP'02, April 6-7, 2002, San Diego, California, USA, pp.61-68				
	S. Khatri, A. Mehrotra, R. Brayton, A. Sangiovanni-Vincentelli, and R. Otten, "A novel VLSI layout fabric for deep sub-micron applications," in <i>Proceedings of the Design Automation Conference</i> , (New Orleans), June 1999.				
	Sunil P. Khatri, Robert K. Brayton, Alberto Sangiovanni-Vincentelli, "Cross-talk Immune VLSI Design using a Network of PLAs Embedded in a Regular Layout Fabric", IEEE/ACM International Conference on Computer Aided Design, ICCAD-2000, November 5-9, 2000, San Jose, CA, USA				
	Sunil P. Khatri, Robert K. Brayton, Alberto Sangiovanni-Vincentelli, "Cross-talk Noise Immune VLSI Design Using Regular Layout Fabrics", Kluwer Academic Publisher: Boston, 2001 (front cover, pages i-xix, 1-51, 95-112 and back cover).	· ·			
		Cite No <sup>1</sup> Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published  Magma Design Automation, Inc., "Deep-Submicron Signal Integrity", white paper, 2002  Andrey V. Mezhiba, Eby G. Friedman, "Scaling Trands of On-Chip Power Distribution Noise", SLIP'02, April 6-7, 2002, San Diego, California, USA, pp.47-53  Sani R. Nassif, Onsi Fakhouri, "Technology Trends in Power-Grid-Induced Noise", SLIP'02, April 6-7, 2002, San Diego, California, USA, pp.55-59  Seongkyun Shin, Yungseon Eo, William R. Eisenstadt, Jongin Shim, "Analytical Signal Integrity Verification Models for Inductance-Dominant Multi-Coupled VLSI Interconnects", SLIP'02, April 6-7, 2002, San Diego, California, USA, pp.61-68  S. Khatri, A. Mehrotra, R. Brayton, A. Sangiovanni-Vincentelli, and R. Otten, "A novel VLSI layout fabric for deep sub-micron applications," in <i>Proceedings of the Design Automation Conference</i> , (New Orleans), June 1999.  Sunil P. Khatri, Robert K. Brayton, Alberto Sangiovanni-Vincentelli, "Cross-talk Immune VLSI Design using a Network of PLAs Embedded in a Regular Layout Fabric", IEEE/ACM International Conference on Computer Aided Design, ICCAD-2000, November 5-9, 2000, San Jose, CA, USA  Sunil P. Khatri, Robert K. Brayton, Alberto Sangiovanni-Vincentelli, "Cross-talk Noise Immune VLSI Design Using Regular Layout Fabrics", Kluwer Academic Publisher: Boston, 2001 (front			

Examiner	Date Considered	
Signature		

<sup>\*</sup>Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

<sup>&</sup>lt;sup>1</sup>Unique citation designation number. <sup>2</sup>Applicant is to place a check mark here if English language Translation is attached.